Schottky diode

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The **Schottky diode** is a two-terminal device consisting of conductive *gate* (for example, a metal) on top of a semiconductor *body*. It is named after Walter H Schottky, who proposed a detailed theory for point contact rectification in 1938.[1] The modern theory of Schottky diode operation was contributed by Hans Bethe (http://nobelprize.org/nobel_prizes/physics/laureates/1967/bethe.html) in 1942.[2] A generic name for this structure is the **metal-semiconductor diode** or **M/S diode**.[3]

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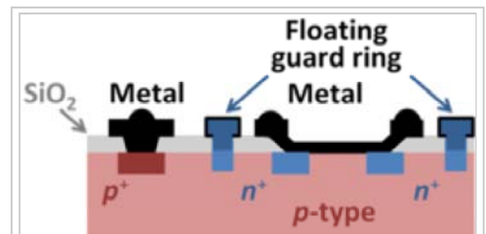
For low voltage applications, below 200V, silicon is used, but for higher voltages (up to 3000 V or more) silicon carbide is used to extend the breakdown voltage. These voltages are achievable only when edge breakdown is avoided, which requires special attention to *edge termination* designs.[4] The figure shows three strategies toward increasing the edge breakdown voltage: an extension of the metal diode contact over a tapered oxide and also an n^+-guard ring and a floating guard ring. These strategies are sometimes used together, but also are used separately.



(PD) Image: John R. Brews

Planar Schottky diode with n^+-guard rings and tapered oxide. The Ohmic contact to the substrate is on the left.

Contact to the body is made through an *ohmic contact* to the *p*-substrate consisting of a metal-to-p^+ region on the surface of the diode. An ohmic contact is one with a linear current-voltage characteristic like that of a resistor.

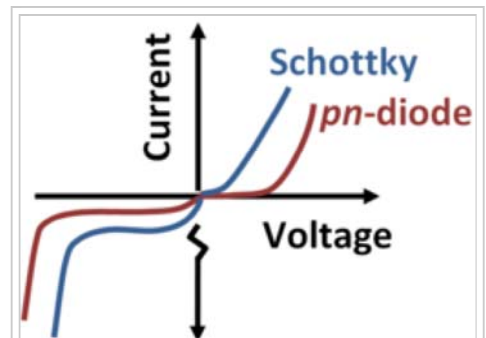
Although the example used in this article is a Schottky diode on a *p*-type substrate, Schottky diodes on *n*-type substrates are more common.

Applications

The Schottky diode is used in a large variety of applications, ranging from practical devices for switching, rectification and photo-detection, to test structures for fabrication monitoring and for studies of semiconductor defects and processes.

Operation

Three different bias cases are examined: zero bias, forward bias, and reverse bias. A simplified one dimensional analysis along a line vertically through the center of the Schottky contact is used throughout. It is imagined that the p^+-ohmic contact is vertically below the Schottky contact.



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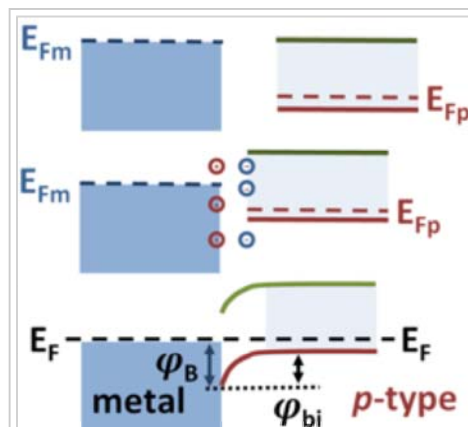
Comparison of Schottky and *pn*-diode current voltage curves.

As seen in the comparison with the *pn*-diode shown in the figure, the Schottky diode tends to turn on at lower forward voltages but rises more slowly because of the nonideality factor noted later. The Schottky diode also tends to have a higher reverse leakage current. The mechanism for current flow is different in the two devices: the *pn*-diode current is diffusion driven by carrier concentration differences, while the Schottky diode is driven by thermionic emission, that is, the surmounting of a potential barrier by energetic carriers. This mechanism is described further below.

Zero bias

Ordinarily, the Fermi levels of different materials differ. When they are brought into electrical contact, enabling electron transfer between the materials, the work done in removing an electron from one material and placing it in the other is equal to the energy difference in the Fermi levels. Consequently, energy is released upon contact by electron transference from the material with the higher Fermi level to the material with the lower Fermi level. This charge transfer continues until the electrical charge difference means the energy gain from transfer is countered by the electrical work required against the

charge difference. At this point the two Fermi levels are brought into coincidence at a common level E_F and no further charge transfer occurs. This flat Fermi level situation corresponds to thermal equilibrium, and no net current flows once equilibrium is reached.



(PD) Image: John R. Brews

Schottky barrier formation on *p*-type semiconductor. *Top*: isolated charge-neutral bulk materials. *Center*: dipole layer formed as materials interact; Fermi level difference is reduced. *Bottom*: final configuration following charge transfer to reach equilibrium with no applied voltage. The neutral (shaded) region in the semiconductor moves away from the interface, leaving a charged depletion region (unshaded) near the interface. Energies are in eV.

The final potential barrier between the metal Fermi level and the majority carrier band edge in the semiconductor is called the *Schottky barrier*, labeled φ_B in the figure. It is a form of contact potential. The concomitant potential drop across the semiconductor depletion layer is called the *built-in* potential, labeled φ_{bi} in the figure.

The formation of a Schottky barrier is shown schematically in the figure, beginning with the isolated materials (top), an intermediate dipole formation stage (center), and the completed configuration with formation of a depletion layer (bottom). The dipole layer still is present in the bottom figure, but is omitted for clarity. The figure is not intended to indicate exactly how the processes occur with increasing proximity of the materials, but merely the processes involved. A more detailed discussion of the figure follows.

The top panel shows a charge-neutral, partly filled metal energy band and a charge-neutral semiconductor valence and conduction band, chemically and electrically isolated from each other. The Fermi level in the *p*-type semiconductor E_{Fp} (assumed to be in units of eV) is near its valence band edge, as set by its acceptor impurity doping. (See Fermi level). The Fermi level in the metal E_{Fm} marks the half-occupancy energy level in the partly filled band of the metal.

The center panel shows schematically the formation of an immobile interfacial dipole layer that alters the Fermi level difference, and adjusts how much mobile charge transfer occurs to form the depletion layer. This dipole formation is not only a result of quantum mechanics at a discontinuity between solids, but chemical processes involving the atomic layers in what is sometimes called the *interface specific region*. The interfacial dipole layer reflects the fact that properties of the bulk materials by themselves do not determine the charge transfer that occurs. Rather, the chemistry of the interface, defects at the interface, and the mechanical adaptation to new atomic positions near the interface that are differently spaced than those found in bulk material, all conspire to alter the amount of charge transfer from that expected from bulk properties.[5] This interface dipole contribution is specific to the interface materials, and is different for (say) a material interface cleaved in vacuum and that for the same material mated to some other material. This interface dipole also is different for differently oriented or differently structured crystal planes. But whatever the final amount of charge transfer, charge transfer occurs and the two adjoined materials each acquire a charge.

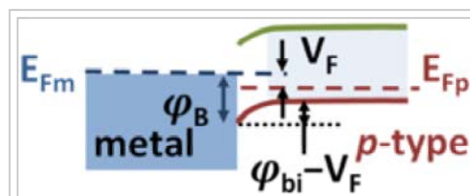
The bottom panel shows the final configuration following mobile charge transfer between the materials. The transfer of electrons from the metal results in a very thin layer of positive charge in the metal very near the interface. Because the electron density in the metal is extremely large, the band bending in the metal is negligible in the diagram. On the other hand, the density of holes in the semiconductor is not nearly as large as the electron density in the metal, so the charging of the semiconductor is spread deeply into the material (the field effect). The semiconductor gains electrons, as indicated by the bending of the valence band edge away from the Fermi level, which increases the valence band occupancy by electrons. Differently stated, the vacancies (holes) in the valence band are reduced in number, and the charge balance in the band-bending region is lost. In this *depletion layer*, the holes or *majority carriers* are depleted (the unshaded surface region in the figure), exposing the immobile negative acceptor dopant ions to make this region charge-negative. This dopant charge results in a potential according to Poisson's equation. The potential decreases with distance toward the bulk semiconductor, and at some distance (the *depletion width*) the bulk properties of the semiconductor are regained and the semiconductor bulk is charge neutral.

At zero bias there is no net current, because the current from the semiconductor is balanced by that from the metal. According to the model of thermionic emission, the current flowing over an energy barrier is proportional to the carrier density next to the barrier. One can imagine the carriers in rapid thermal motion randomly directed. The carriers approaching the barrier with energies lower than the barrier height bounce off the barrier and do not cross it. Some fraction of those that are more energetic escape backward scattering to succeed in surmounting the barrier, and are lost to the far side. On the metal side, hole injection from the metal Fermi level into the semiconductor valence band is small as it requires surmounting a large energy barrier. On the semiconductor side, hole injection into the metal requires surmounting the built-in barrier height, φ_{bi}. Although the barrier on the semiconductor side is smaller than the Schottky barrier φ_B on the metal side, so is the carrier

density. The two currents balance at zero bias, so no net current flows. These balancing current flows are much larger than in the *pn*-diode because thermionic emission results in larger currents than the diffusion-recombination mechanism of the *pn*-diode.[6]

Evidently the interface specific region between the metal and the semiconductor determines the Schottky barrier height φ_B. While this barrier height is very influential in determining the current, other interfacial properties also help to decide just how much current will be injected at a given barrier height, sometimes lumped into a factor called the "generalized Richardson constant", named after the Nobel Prize winning author of the original theory of thermionic emission, Owen Willans Richardson (http://nobelprize.org/nobel_prizes/physics/laureates/1928/richardson.html). However, in real devices thermionic emission is complicated by the effects of diffusion, barrier shape, field emission, homogeneity of the interface, and so forth.[7] Calculation of the barrier height based upon a fundamental understanding either of current balance or of charge transfer should lead to the same result, but at present such detailed calculations remain topics for research.

Forward bias



(PD) Image: John R. Brews

Under forward bias V_F the potential drop across the depletion layer is reduced, the depletion region is narrower, and the Fermi levels are split.

Under forward bias, a net current of holes now flows from the semiconductor to the metal (or, equivalently, of electrons from the metal to the semiconductor). At zero bias there is no net current, because the current from the semiconductor is balanced by that from the metal. But under forward bias the current from the metal side is unaffected (and extremely small), while that on the semiconductor side is increased by the forward bias, as discussed next.

If a forward bias voltage is applied V_F, the Fermi level of the bulk metal E_{Fm} (in eV) is raised in energy above the bulk Fermi level in the semiconductor E_{Fp}, which lowers the potential drop across the depletion layer to a value $\varphi_{bi}-V_F$ and increases the hole current from the semiconductor to the metal. In contrast to the lowered barrier on the semiconductor side, the alignment of the metal Fermi level relative to the semiconductor band edges at the interface is not changed by the bias: that is, φ_B is fixed by the processes involved in adjusting the Fermi levels to achieve equilibrium at zero applied bias. That fixed alignment means the barrier for hole injection from the metal into the semiconductor is not changed by an applied bias, and the injected hole current from the metal remains the same as at zero bias.

According to the model of thermionic emission, the electrical current injected from the semiconductor is proportional to the hole density at the interface. Using a simple Boltzmann approximation to the Fermi function, the hole density on the semiconductor side is increased under forward bias by a factor:

$p(V_F) = p(0)e^{qV_F/k_BT} \ ,$

where *p(0)* is the zero forward bias value of hole density on the semiconductor side. The hole current from the semiconductor to the metal therefore is increased by this factor. The current, being by convention a flow of positive charge, is therefore positive from the semiconductor to the metal, and the Schottky barrier current in forward bias becomes:

$I(V_F) = I(0)\left(e^{qV_F/k_BT}-1 \right) \ ,$

where *I(0)* is related to the zero-bias current exchange between the two materials.

Due to some complications of real Schottky barriers, for example, inhomogeneity (patchwork) of the interface or intervening contamination layers, the current is usually represented as:[8]

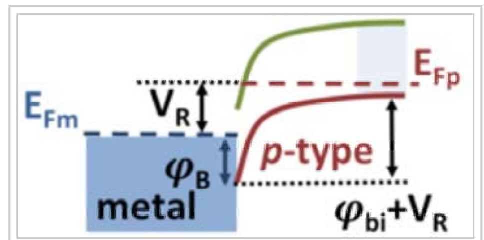
$I(V_F) = I(0)\left(e^{qV_F/nk_BT}-1 \right) \ ,$

where the factor n is called the *ideality factor*, and is usually in the range 1 - 2.

Reverse bias

If a reverse bias V_R is applied, the Fermi level of the metal is lowered below that of the semiconductor, and the barrier height for holes is increased on the semiconductor side by the amount of the reverse bias. The hole density is therefore decreased compared to equilibrium (the electron occupancy increases) and the current from the semiconductor falls below the equilibrium value. That means the diode current changes direction compared to the forward biased case.

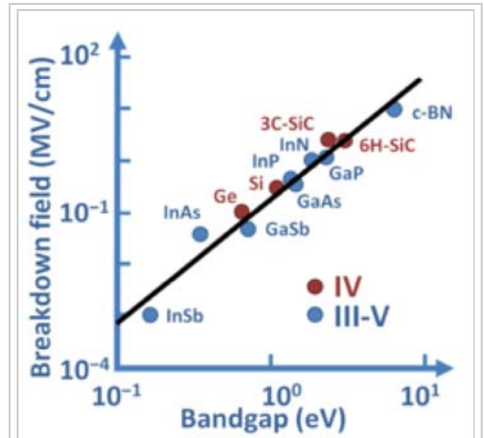
If the diode were ideal, the current in reverse bias would be simply *−I(0)*, the hole current backward injected by the metal into the semiconductor at zero bias, because the the hole current from the semiconductor side is completely suppressed by the very low hole density at the interface in reverse bias, making the injection of holes into the metal nearly zero. However, in practice, in reverse bias a leakage current is drawn due to generation of electrons and holes by defects in the depletion layer. If a large enough reverse voltage is applied, breakdown occurs, due to runaway of the generation mechanisms, or more commonly, due to edge breakdown in the high field region near the contact perimeter. A brief outline of the breakdown phenomena follows.[9]



(PD) Image: John R. Brews

Schottky diode under reverse bias V_R. The potential drop across the depletion layer is increased, and the depletion layer is widened by the reverse bias.

Under reverse bias, a large electric field is present in the depletion layer, and carriers in the depletion layer are accelerated by this field. The carriers gain energy from the field, but they lose energy by creating vibrations in the semiconductor lattice, called *phonons*, thereby heating up the material. However, as the field increases with application of a larger reverse bias voltage, an increased fraction of the high energy carriers fail to lose energy by phonon creation, attaining energies in excess of the material bandgap. These energetic carriers, instead of losing energy to phonons, lose energy by creating electron-hole pairs, a process called *impact ionization*. At a crucial *breakdown field*, these generated carrier pairs themselves generate pairs and the process enters runaway.



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Critical electric field for breakdown *versus* bandgap energy in several materials.

A wider bandgap material like SiC has a higher intrinsic breakdown voltage than a lower bandgap material like Si because the energy to make an electron-hole pair scales with the bandgap. An electron created by impact ionization is in the conduction band, and the associated hole is in the valence band, and these two are separated in energy by at least the bandgap energy. This bandgap energy is provided by the electric field inside the depletion layer, which must accelerate the impacting carrier beyond this energy before generation can occur. The figure shows a log-log plot of field upon the bandgap energy fitted to an empirical power law with exponent 2.4.[10]

Unlike the MOSFET or the MOS capacitor, the expansion of the depletion layer width in response to an applied reverse bias is not arrested at large biases by formation of an inversion layer, a thin surface layer at the interface made up of minority carriers (electrons in a *p*-type semiconductor). An inversion layer cannot form, because the carriers are transmitted to the metal, and cannot be stored at the interface.

Transient response

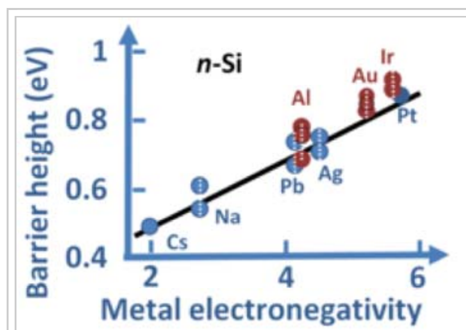
A Schottky diode in forward bias conducts a current. This current can be cut off by switching to a reverse bias. The response time of the diode is simply the time it takes for the holes to move back from the edge of the narrow depletion region of forward bias to the edge of the wider depletion region of reverse bias. This switching is very rapid, the switching time given by the *RC* time constant of the diode, where *R* is the resistance of the bulk *p*-type material and its ohmic contact, and *C* is the diode capacitance. To understand the nature of this capacitance, note that the majority carriers in the semiconductor (holes in this example) are separated from the metal contact by the insulating depletion layer, where there are only immobile dopant ions, and no mobile carriers. Thus, the diode represents an electric capacitor with two plates, namely the metal and the neutral bulk material, separated by a dielectric, namely the insulating depletion region.

Compared to the MOS capacitor, or the pn-diode or the bipolar transistor, this switching time is very fast because it is not limited by the response time of minority carriers, which have to be removed from those devices by slow recombination processes.

Barrier height

From the very earliest work of Schottky, Mott and Davydov it was expected that the Schottky barrier height would depend upon the electronegativity of the metal contact, as that measures the tendency of the metal to grab electrons. The more electronegative the metal, the more it will resist transfer of electrons to the semiconductor (other factors being equal). For a *p*-type semiconductor, transfer of electrons is between the metal and the valence band of the semiconductor, and a greater electronegativity of the metal means fewer electrons for the semiconductor, or a lower barrier against hole injection from the

metal to the valence band. For an *n*-type semiconductor, a greater electronegativity of the metal means fewer electrons for the conduction band of the semiconductor, and a higher barrier against electron transference out of the metal into the conduction band.



(PD) Image: John R. Brews

Schottky barrier height *vs.* metal electronegativity for some selected metals on *n*-type silicon. The straight line is a theoretical result based upon one theory of interface dipole formation, the theory of metal induced gap states.

The figure shows the Schottky barrier against injection of electrons into the conduction band of *n*-type Si as a function of electronegativity of the metal. A correlation with electronegativity is observed, but the dependence is not as strong as originally thought because of the influence of the details of the interface charge distribution.[11] The theoretical straight line is:

$\varphi_B = 0.76 +0.101 (X_m-X_{Si}) \ ,$

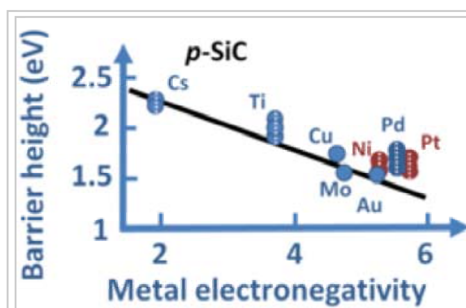
where all units are in eV, X_m is the Miedema electronegativity of the conducting contact, and X_{Si} is the Miedema electronegativity of silicon. [12] The slope of 0.101eV/Miedema electronegativity unit can be compared with the original Schottky-Mott rule, which focused upon properties of the metal and semiconductor viewed in isolation, leading to a barrier given by:

$\varphi_B = \Phi_M-\chi_S \ ,$

where Φ_M is the metal workfunction (energy to remove an electron from the metal) and χ_S is the semiconductor electron affinity (ionization energy of semiconductor). This equation leads to a slope of about 1eV/Miedema unit, much larger than the slope in the figure.

The figure also shows multiple barrier heights for the same metal are observed, corresponding to different interface structures.

Different semiconductors will lead to different slopes for such a plot. An example for diodes on *p*-type SiC is shown in the figure.[13] The slope of the theoretical straight line in this figure is −0.24eV/Miedema electronegativity unit. A negative slope is expected for *p*-type semiconductors (ignoring other factors) because the more electronegative the metal the fewer electrons it will transfer to the valence band of the semiconductor, or differently stated, the lower the barrier height for hole injection into the semiconductor.



(PD) Image: John R. Brews

Theoretical dependence of Schottky barrier heights for diodes using *p*-SiC *vs.* electronegativity of the metal according to Mönch[13]

The theory behind the low slopes of the straight lines in the figures is based upon dividing electronic states at the metal semiconductor interface into four groups: (i) electron states in the metal, called the metal-induced gap states (MIGS), which have an amplitude that decays into the semiconductor (ii) electron states in the semiconductor that decay into the metal, (iii) localized states that decay from the interface both into the metal and into the semiconductor, and finally (iv) those states that are bulk-like in both materials and decay in neither one. The theory plotted in the figure, the MIGS theory, suggests that the barrier height is determined primarily by the first group of states.[11] The original identification of these states, also known as *interface-induced gap states* (IFIGS), was made by Heine at Bell Labs.[14] A simplified version of this model predicts an interface charge dipole that results from the negative charge in the MIGS and the positive image charge reflected in the metal itself. This interface dipole is found to be influenced by the metal electronegativity (as is the entire chemistry of the interface specific region), but has a weaker dependence upon electronegativity than proposed by the simple Schottky-Mott rule.

The role of MIGS in explaining the interface dipole in the interface specific region is still under discussion, and alternatives are proposed like the *bond polarization model* with its origins in molecular studies. An overview and assessment of these theories is provided by Tung, who emphasizes that the MIGS are an interface property and depend upon both the metal and the semiconductor.[15]

Whatever the underlying origin of the interface dipole, it reduces the initial mismatch between the semiconductor and the metal Fermi levels, reducing the amount of mobile charge transfer that creates the depletion layer, thereby reducing the built-in potential drop in the semiconductor and reducing the depth of the depletion region.

Notes

1. ↑ W. Schottky (1939). "Zur Halbleitertheorie der Sperrschicht- und Spitzengleichrichter". *Zeitschrift für Physik A Hadrons and Nuclei* **vol. 113**: pp. 813 *ff*. DOI:10.1007/BF01340116 (http://dx.doi.org/10.1007/BF01340116). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1007/BF01340116). W. Schottky (1941). "Vereinfachte und erweiterte Theorie der Randschicht-gleichrichter". *Zeitschrift für Physik A Hadrons and Nuclei* **vol. 118**: pp. 539 *ff*. DOI:10.1007/BF01329843 (http://dx.doi.org/10.1007/BF01329843). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1007/BF01329843). See also E. Spenke (1949). "Zur Randschichttheorie der Trockengleichrichter". *Z. Physik* **vol. 126**: pp. 67 *ff*. DOI:10.1007/BF01331042 (http://dx.doi.org/10.1007/BF01331042). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1007/BF01331042).
2. ↑ HA Bethe (November, 1942). "MIT Radiation Lab. Report" **vol. 43-12**.
3. ↑ The term "Schottky diode" may be taken erroneously to refer to diffusion as the mechanism of operation as first proposed by Mott, Schottky and Davydov. However, the mechanism in most devices is a combination of thermionic emission and diffusion, as later proposed by Bethe, the so-called *thermionic-diffusion* theory. See Chih-Tang Sah (1991). "§560: Metal/semiconductor diode", *Fundamentals of solid-state electronics (http://books.google.com/books?id=205wsYbl2fAC&pg=PA474)*. World Scientific, p. 474. ISBN 9810206372. and SM Sze and KK Ng (2007). "Chapter 3 Metal-semiconductor contacts", *Physics of semiconductor devices (http://books.google.com/books?id=zHh-z5vZ7ZoC&pg=PA134)*, 3rd ed. Wiley, pp. 134 *ff*. ISBN 0471143235.
4. ↑ B. Jayant Baliga (2005). "§3.2 Schottky diode edge terminations", *Silicon carbide power devices (http://books.google.com/books?id=LNLVwAzhN7EC&pg=PA44)*. World Scientific, pp. 44 *ff*. ISBN 9812566058.
5. ↑ For further discussion, see for example, Howard R. Huff, H. Iwai, H. Richter (2006). "Electrical properties: Partial charge transfer in interface bonds", *Silicon Materials Science and Technology X, Issue 2 (http://books.google.com/books?id=KqIa5SCP93sC&pg=PA195#v=onepage&q&f=false)*. The Electrochemical Society, p. 195. ISBN 156677439X. Raymond T Tung (2001). "Recent advances in Schottky barrier concepts" (http://www.sciencedirect.com/science?_ob=ArticleURL&_udi=B6TXH-43VKKX9-1&_user=9555371&_coverDate=11%2F09%2F2001&_rdoc=1&_fmt=high&_orig=search&_origin=search&_s *Materials Science and Engineering: R: Reports* **vol. 35** (1-3): pp. 1-138. DOI:10.1016/S0927-796X(01)00037-7 (http://dx.doi.org/10.1016/S0927-796X(01)00037-7). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1016/S0927-796X(01)00037-7). David Cahen, Gary Hodes (2002-06-05). "Molecules and electronic materials" (http://onlinelibrary.wiley.com/doi/10.1002/1521-4095%2820020605%2914:11%3C789::AID-ADMA789%3E3.0.CO;2-H/abstract). *Advanced materials progress report* **vol. 14** (No. 11): pp. 789-798. DOI: (http://dx.doi.org/) 10.1002/1521-4095(20020605)14:11<789::AID-ADMA789>3.0.CO;2-H
6. ↑ See the discussion in the general reference by CT Sah, p. 489.
7. ↑ Raymond T Tung (November 2001). "Recent advances in Schottky barrier concepts". *Materials Science and Engineering: R: Reports* **vol. 35** (Nos. 1-3): pp. 1-138. DOI:10.1016/S0927-796X(01)00037-7 (http://dx.doi.org/10.1016/S0927-796X(01)00037-7). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1016/S0927-796X(01)00037-7).
8. ↑ The ideality factor for Schottky diodes is discussed extensively by Winfried Mönch (2010). "§3.5 Barrier heights of real Schottky contacts", *Electronic Properties of Semiconductor Interfaces (http://www.amazon.com/Electronic-Properties-Semiconductor-Interfaces-Springer/dp/3642057780/ref=tmm_pap_title_0?ie=UTF8&qid=1297449649&sr=1-1#reader_3642057780)*. Springer, pp. 47 *ff*. ISBN 3642057780.
9. ↑ A discussion is found, for example, in Yuan Taur, Tak H Ning (2005). "§2.4 High-field effects", *Fundamentals of modern VLSI devices (http://www.amazon.com/Fundamentals-Modern-VLSI-Devices-Yuan/dp/0521559596/ref=sr_1_1?s=books&ie=UTF8&qid=1296846816&sr=1-1#reader_0521559* Cambridge University Press, pp. 90 *ff*. ISBN 9780521559591.
10. ↑ Sadao Adachi (2005). "Figure 9.11", *Properties of group-IV, III-V and II-VI semiconductors (http://books.google.com/books?id=1h66hZXADTMC&pg=PA206)*. Wiley. ISBN 0470090324.
11. ↑ [11.0] [11.1] Winfried Mönch (2001). "Figure 19.18", *Semiconductor Surfaces and Interfaces (http://www.amazon.com/Semiconductor-Surfaces-Interfaces-Winfried-M%C3%B6nch/dp/3540679022/ref=sr_1_1?s=books&ie=UTF8&qid=1297043881&sr=1-1#reader_354067*9 3rd ed. Springer, p. 412. ISBN 3540679022.
12. ↑ The Miedema electronegativity unit is derived from the work functions of metal alloys and intermetallic compounds, and is thought to be more appropriate here than the electronegativity scale of Pauling based upon covalent bonds in small molecules. See A.R. Miedema (July,1973). "The electronegativity parameter for transition metals: Heat of formation and charge transfer in alloys". *Journal of the less common metals* **vol. 32** (No. 1): pp 117-136. DOI:10.1016/0022-5088(73)90078-7 (http://dx.doi.org/10.1016/0022-5088(73)90078-7). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1016/0022-5088(73)90078-7). The Miedema scale is related to Pauling's scale approximately as $X_{Mied} = 1.93X_{Paul} + 0.87$, according to W. Mönch (2006). "Equation (2.16)", Susanne Siebentritt, Uwe Rau, eds: *Wide-gap chalcopyrites (http://books.google.com/books?id=9Hy2L3gYBBMC&pg=PA24)*. Birkhäuser, p. 24. ISBN 3540244972. A tabulation of Miedema electronegativites is found in AR Miedema (1992). "Energy effects and charge transfer in metal physics: modelling in real space". *Physica B: Condensed Matter* **vol. 182**: p. 14. DOI:10.1016/0921-4526(92)90565-A (http://dx.doi.org/10.1016/0921-4526(92)90565-A). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1016/0921-4526(92)90565-A). Some particular values are: $X_{Si} = 4.7$, $X_{Cs} = 1.95$, $X_{Pt} = 5.65$.
13. ↑ [13.0] [13.1] Figure adapted from Winfried Mönch (2004). "Figure 9", W. J. Choyke, Hiroyuki Matsunami, Gerhard Pensl, eds: *Silicon carbide: recent major advances (http://books.google.com/books?id=mLBmKotEe9cC&pg=PA319)*. Springer, p. 139. ISBN 3540404589.
14. ↑ V. Heine (1965). "Theory of surface states" (http://link.aps.org/doi/10.1103/PhysRev.138.A1689). *Phys. Rev.* **vol. 138**: pp. A1689-A1696. DOI:10.1103/PhysRev.138.A1689 (http://dx.doi.org/10.1103/PhysRev.138.A1689). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1103/PhysRev.138.A1689).
15. ↑ Raymond T Tung (2001). "Previously cited paper; §4: Models on bonds and dipoles at MS interfaces" (http://www.sciencedirect.com/science?_ob=ArticleURL&_udi=B6TXH-43VKKX9-1&_user=9555371&_coverDate=11%2F09%2F2001&_rdoc=1&_fmt=high&_orig=search&_origin=search&_ *Materials Science and Engineering: R: Reports* **vol. 35** (1-3): pp. 1-138. DOI:10.1016/S0927-796X(01)00037-7 (http://dx.doi.org/10.1016/S0927-796X(01)00037-7). Research Blogging (http://researchblogging.org/post-search/list?search_text=10.1016/S0927-796X(01)00037-7).

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